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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 65913 | 7590 | 09/03/2009 | EXAMINER | |
| NXP, B.V. | | | LANGMAN, JONATHAN C | |
| NXP INTELLECTUAL PROPERTY & LICENSING | | | | |
| M/S41-SJ | | | ART UNIT | PAPER NUMBER |
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| SAN JOSE, CA 95131 | | | | |
| NOTIFICATION DATE | | DELIVERY MODE | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/539,260 | HAISMA, JAN | |
| | Examiner | Art Unit | |
| | JONATHAN C. LANGMAN | 1794 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 19 May 2009.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-10 and 21-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10 and 21-28 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 and 21-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation.

In regards to claims 1- 5, Haberger et al. teach an SOI wafer comprising a first substrate and a second substrate bonded to each other by their faces via one or several intermediate bonding layers. At least one of the bonding layers is configured that it presents recesses (col. 3, lines 62-66). The two substrates are preferably semiconductor substrates (col. 4, lines 5), and specifically mention the substrates to be silicon (see the entire specification). As seen in Figure 3, in the first picture of the cross section views of group 5, the substrate exhibits pillars that extend from the substrate. Haberger teaches "Where the structures may be performed also as far as into the substrate as such" (col. 7, lines 45-50). Haberger teaches rounded corners (col. 4, lines 40-53 or col. 7, lines 35-40). These rounded corners naturally occur during forming the structures through wet etching. The trenches are formed of the same material and by

the same process as instantly claimed (selective patterning with photolithography and then wet or dry etching), and therefore are expected to have the same structural features as instantly claimed.

Two silicon wafers will have dilatation behaviors that are substantially the same, since they are the same material. The bonding layers are taught to be SiO₂ in preferred embodiments (col. 5, lines 1-8). A SiO₂ layer has a dilatation mismatch with the first layer (silicon). The patterned trenches are structures that expectantly and inherently absorb stress originating from the dilatation mismatch.

Since Haberger teaches the same structure as instantly claimed, it is expected to behave in the same manner as instantly claimed. It has been held that where the claimed and prior art products are identical or substantially identical in structure or are produced by identical or a substantially identical processes, a *prima facie* case of either anticipation or obviousness will be considered to have been established over functional limitations that stem from the claimed structure. *In re Best*, 195 USPQ 430, 433 (CCPA 1977), *In re Spada*, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). The ***prima facie*** case can be rebutted by evidence showing that the prior art products do not necessarily posses the characteristics of the claimed products. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Even though Haberger teaches a subsequent step of introducing etchants in between the two silicon layers through the recesses in order to separate the structures. The intermediate layer as formed will read on the applicants structure as instantly claimed, and still qualifies as prior art.

Regarding claim 6, SiO₂ is electrically insulating.

Regarding claim 7, Haberger et al. teaches that the width of the trenches and height of the trenches is less than one centimeter (col. 6, lines 61-64).

Regarding claim 8, the channels have a linear orientation perpendicular to a plane of the carrier (col. 4, lines 38-39, and figures 2).

Regarding claim 9, the channels are rectangular in shape and extend across the wafer (figure 2), therefore, the structures are parallel to a plane of the carrier. Furthermore, Haberger et al. describe that the structures need not present a rectangular cross section, or across linear orientations (col. 4, lines 38-43), Haberger teaches the shapes of the channels may be rounded, rectangular or polygonal (col. 7, lines 35-40).

Regarding claim 10, the composite substrate is an SOI wafer.

Regarding claims 21 and 23, the layers are all bonded to each other (col. 3, lines 60-65).

Regarding claim 22, the wafers of Haberger et al are silicon (semiconductor material) and the intermediate layer is silicon oxide 9oxide of the semiconductor material) (see at least (col. 5, lines 1-5, and col. 2, lines 25-35).

Regarding claims 24, Haberger teaches an oxide layer present atop a silicon wafer but is silent to the means of achieving this layer, specifically thermally oxidizing the surface of the semiconductor wafer. However, Haberger teaches the same materials and the same structure, and therefor, the process limitations are given little patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The

patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.", (In re Thorpe, 227 USPQ 964,966). Once the Examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product (In re Marosi, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983), MPEP 2113).

Regarding claims 25 and 26, the structure of Haberger is the same as instantly claimed, and Haberger teaches placing the structures at selected locations of the intermediate layer (see the figures). For these reasons it is the examiner's position that since Haberger teaches the same materials, the same structures, and the same spacing, that they will inherently and expectedly possess the same characteristics of stress relief as instantly claimed, and removing dislocations as instantly claimed. Stress is expected to occur between the mismatched layers, and since Haberger teaches the same structures as instantly claimed and the same position of the intermediate layer as instantly claimed, the structures of Haberger are said to be located at least where there is some degree of stress originating from the dilatation mismatch. See in re best applied above.

Regarding claim 27, Haberger teaches that the structures may be in the form of islets (col. 7, lines 49-60) and may have a round structure (col. 7, lines 35-40). The

widths of the structures are taught to be 0.1 microns to 2 microns (col. 4, lines 10) thereby showing a diameter in the range instantly claimed.

Regarding claim 28, Haberger teaches a device layer formed on the thinned semiconductor (col. 6, lines 25-30) and col. 5 lines 30-35), which is preformed before the separation of the structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 27 are rejected under 35 U.S.C. 103(a) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation, as applied above.

Haberger et al. teach a SOI substrate comprising two semiconductor wafers separated by a patterned oxide insulating layer of silicon dioxide, as described above. Haberger et al. teach shapes and sizes as seen in figures 2 and 3, and mentioned above, in which rounded structures in an islet form are mentioned. Haberger also teaches that the widths of the structures are between 0.1 and 2 microns. Haberger does not mention the exact sizes and shapes as instantly claimed, however it would have been obvious to a person having ordinary skill in the art at the time the present invention was made, and well within their grasp, to choose any desired pattern including

those shapes and sizes instantly claimed, as these are shown to be desired effective results. It would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the shapes and sizes of patterns in the insulating layer for the intended application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

The applicant argues that Haberger does not teach rounded corners in the cited passage (col. 4, lines 40-47). The Examiner previously relied on the fact that wet etching would necessarily result in rounded corners. The Examiner directs the applicant to claim 1 of US 2001/0023960 to further support this position. If the applicant still refutes that wet chemical etching does not result in rounded corners, then the Examiner directs the applicant to the passages below.

To further support the Examiners position that the corners forming the pillars may be rounded the Examiner directs the applicant to Haberger, col. 7, lines 35-40 and the channel cross section figures shown in Figure 3. Haberger teaches that exemplary shapes of the channels are rectangular structures, round, meandering or polygon type structures. Figure 3 shows rectangular and polygon type structures. In looking at Figure 3, one of routine skill in the art would immediately envisage the other two structures, rounded and meandering, as the shape for the channels shown in Figure 3.

This teaching of round channel shapes, accompanied with Figure 3, provides sufficient specificity to anticipate the rounded corners instantly claimed.

The applicant argues that the first channel pictured in Figure 3, (the only figure that shows a structure formed into the substrate) has straight edges, and does not comprise rounded corners. However, “applicant must look to the whole reference for what it teaches. Applicant cannot merely rely on the examples and argue that the reference did not teach others.” In re Courtright, 377 F.2d 647, 153 USPQ 735,739 (CCPA 1967). Haberger teaches that among rectangular shaped channels, exemplary shaped channels comprise round and meandering shaped structures. One would immediately envisage a round channel shape, as this is only one of three alternatives channel shapes disclosed by Haberger.

The round shaped cross sections will necessarily have a gradual interface between the sidewalls of the pillar extensions and the surface of the carrier. And also will inherently and intrinsically reduce stress originating from the dilatation mismatch (Haberger col. 7, lines 54 and 55, as well as col. 8, lines 15-23).

Regarding the applicant’s arguments to claim 24, The Examiner had already established in the rejection that the intermediate layer is a semiconductor oxide (page 3 paragraph starting with “two silicon wafers” and in rejecting claim 6 on page 4 of the rejection). The product by process case law was used to reject claim 24, because Haberger although teaching a semiconductor oxide as an intermediate layer, does not specifically teach forming the semiconductor oxide layer through thermal oxidation. The office never acknowledges that Haberger does not teach a semiconductor oxide. The

office only acknowledges that Haberger fails to teach that the semiconductor oxide layer is formed by thermal oxidation.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN C. LANGMAN whose telephone number is (571)272-4811. The examiner can normally be reached on Mon-Thurs 8:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on 571-272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCL

/Timothy M. Speer/
Primary Examiner, Art Unit 1794